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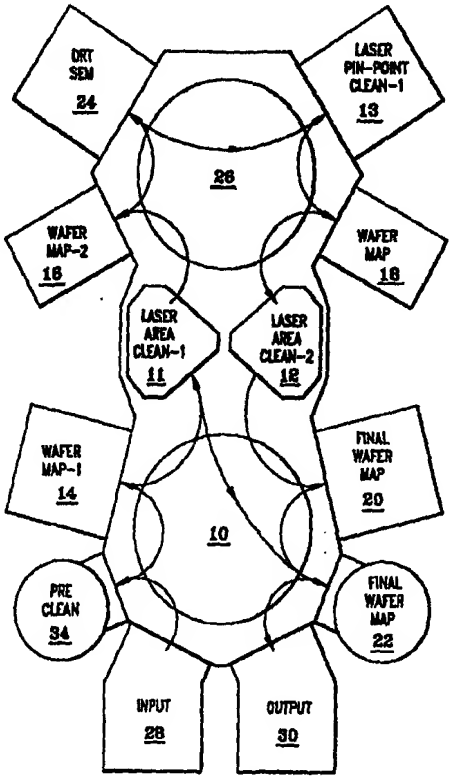
(54) Title: SEMICONDUCTOR WAFER PROCESSING APPARATUS AND METHOD WITH DEFECT ERADICATION

(57) Abstract

An improved semiconductor wafer processing apparatus (10) includes a series of processing stations combined in one form, coupled together by computer-controlled cluster tooling to achieve a selected defect level in the range of 0.01 defects/cm$^2$ or fewer. Wafers are supplied in a pod to an input station (28) which initiates a data record for recording processing results at each station. Individual wafers are transferred to a computer-controlled defect-mapping station (14) where defects are identified and their position coordinates recorded. Defect-mapped wafers are transferred to a computer-controlled laser area cleaning station (11) which lifts the defects and sweeps the wafer surface clean, except for stubborn defects. Clean wafers are transferred to a final mapping station (20 or 22), followed by transfer of the wafers to an output station (30). Wafers including stubborn defects are transferred to a second defect-mapping station (16) where stubborn defects are located by coordinates, after which the wafers are transferred to a Defect Review Tool incorporating a Scanning Electron Microscope (SEM-DRT) (24). A SEM image review of stubborn defects includes chemical analysis of the stubborn defects. A laser point-cleaning station (13) lifts and sweeps each stubborn defect individually from the wafer surface. Cleaned wafers are transferred to a third defect-mapping station (18) for recording any stubborn defects remaining, then to a second laser area cleaning station (12) for a final cleaning, followed by transfer of the wafers to a final mapping station (20 or 22) for mapping of any remaining stubborn defects. The accompanying data records are updated followed by transfer of the wafers to an output station (30).



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**Title of Invention**

# SEMICONDUCTOR WAFER PROCESSING APPARATUS AND METHOD WITH DEFECT ERADICATION

## DESCRIPTION

### Cross-reference to related application

This application is related to U.S. provisional patent application Ser. No. 60/047,907 filed in the United States Patent and Trademark Office on 29 May 1997.

### Technical Field

This invention relates to manufacturing methods and apparatus. More particularly, the invention relates to manufacturing methods and apparatus for defect eradication on semiconductor wafers and the like.

### Background Art

The semiconductor industry is moving into the 21st century with accelerating technological speed driven by small feature sizes and large wafers. This advanced technology capability will become increasingly more difficult to harness and more costly to implement. The Semiconductor Industry Association (SIA) Road map projects that the 0.18 micron/300mm wafer technology generation in 2001 will require a level of 0.01 defects/$cm^2$ to produce high yield IC products. Not only is this density very low (2/3 defects per 300 mm wafer), but particles as small as 0.06 micrometer (approximately 100 atoms) in diameter can cause electrical IC product failures. Low defect levels are critical for economic success in the IC industry. Table 1 illustrates the effect of defect density level on test yield for several 0.18 micron products: A dynamic RAM memory (DRAM) of 1 Gigabits per chip, a 1000 MIP microprocessor, and a system-on-a-chip IC product (SOC). An increase of defect density (microprocessor) from 0.01 D/$cm^2$ to 0.05 D/$cm^2$ reduces the test yield from 70% to 12%. The IC industry's future economic success will have strong dependency on its ability to develop technology of tool systems that maintain very low defect levels, even as the industry produces finer and finer feature sizes. This

yield analysis focuses on three products: DRAM, microprocessor, and system on a chip. Test yields were rigorously calculated for these three products and three technology generations --- 0.35 micron, 0.25 micron, and 0.10 micron. Table 2 illustrates the specific yields utilized in the study. The IC industry needs technology tools that will eradicate defects in order to achieve the very low defect levels required, even as the industry produces finer and finer feature sizes.

Surface contaminant defects include discrete pieces of matter that range in size from submicron dimension to granules visible to observation with the eye. Such contaminants may be fine dust, dirt particles, or unwanted molecules comprised of elements such as carbon, hydrogen, and/or oxygen. Particulate contaminants ("particulates") frequently adhere to a surface by weak covalent bonds, electrostatic forces, van der Waals forces, hydrogen bonding, coulombic forces, or dipole-dipole interactions, making removal of the particulates difficult. Particulates frequently encountered in practice include polysilicon slivers, photoresist particles, metal oxide particles, metal particles, and slurry residue. It is known that not all particulates are equally undesirable. For example, particulates that adhere at some non-sensitive portions of the IC circuitry may have no effect on operation or performance, and need not necessarily be removed ("don't cares"). On the other hand, particulates that adhere at critical locations ("killer defects") can cause failure of the IC circuitry and must be removed for proper operation. In certain instances, the presence of surface contaminants renders the contaminated substrate less efficient or inoperable for the substrate's designated purpose. In semiconductors, surface defects due to minor molecular contaminants often render semiconductor masks or chips worthless. As shown by Tables 1 and 2 above, reducing the number of molecular surface defects on a semiconductor wafer by even a small amount can radically improve semiconductor chip test yields. Similarly, removing molecular surface contaminants, such as carbon or oxygen, from the surface of silicon wafer circuit layers as deposited on the wafer or between deposition of layers significantly improves the quality of the IC chip produced.

**Table 1**

| Product | Defect Density | Test Yield |
|---|---|---|
| 1 Gigabit DRAM | 0.01 Defect/$cm^2$ | 81% |
| 1 Gigabit DRAM | 0.03 Defect/$cm^2$ | 53% |
| 1 Gigabit DRAM | 0.10 Defect/$cm^2$ | 12% |
| Microprocessor (1000 MIP) | 0.01 Defect/$cm^2$ | 70% |
| Microprocessor (1000 MIP) | 0.03 Defect/$cm^2$ | 28 % |
| Microprocessor (1000 MIP) | 0.05 Defect/$cm^2$ | 12 % |
| System on a Chip (SOC) | 0.01 Defect/$cm^2$ | 64% |
| System on a Chip (SOC) | 0.03 Defect/$cm^2$ | 25 % |
| System on a Chip (SOC) | 0.04 Defect/$cm^2$ | 12% |

**Table 2**

| Product | Size | Defect/cm$^2$ | Maximum Yield |
|---|---|---|---|
| 64 M DRAM | 0.35 micrometer | 0.05/cm$^2$ | 67% |
| 200 MIP Microprocessor | 0.35 micrometer | 0.05/cm$^2$ | 42% |
| SOC | 0.35 micrometer | 0.05/cm$^2$ | 27% |
| 256 DRAM | 0.25 micrometer | 0.03/cm$^2$ | 70% |
| 600 MIP Microprocessor | 0.25 micrometer | 0.03/cm$^2$ | 46% |
| SOC | 0.25 micrometer | 0.03/cm$^2$ | 35% |
| 1 G DRAM | 0.18 micrometer | 0.01/cm$^2$ | 81% |
| 1000 MIP Microprocessor | 0.18 micrometer | 0.01/cm$^2$ | 70% |
| SOC | 0.18 micrometer | 0.01/cm$^2$ | 64% |

The need for clean surfaces, free of even the finest contaminants, has led to the development of a variety of currently used surface cleaning methods. These known methods, however, each have their own serious drawbacks. For example, widely used chemical and mechanical cleaning techniques require the use of cleaning tools and agents that can introduce as many new contaminants to a treatment surface as they remove. Another currently used method for cleaning substrate surfaces without outside agents requires that the treatment surface be melted to release contaminants which are then removed by ultra high vacuum pressure. This method has the disadvantage that the surface being treated must be briefly melted, which may be undesirable, as for example, when a semiconductor surface is cleaned between deposition of circuit layers and it is desired that the integrity of the previously deposited layers not be disturbed. A further disadvantage with this process is that ultra high vacuum equipment is both expensive and time consuming to operate. Annealing treatment methods suffer similar drawbacks. When a surface is cleaned by annealing methods, the treatment surface of the substrate being cleaned is heated to a temperature that is generally below the melting point of the material being treated but high enough to enable rearrangement of the material's crystal structure. The surface being treated is held at this elevated temperature for an extended period during which time the surface molecular structure is rearranged and contaminants are removed by ultra high vacuum. Annealing cleaning methods cannot be used where it is desired to preserve the integrity of the existing structure being cleaned.

Another currently utilized cleaning method, known as ablation, suffers from its own particular drawbacks. With ablation, a surface or contaminants on a surface are heated to the point of vaporization. Depending on the material being ablated, the material may melt before being vaporized, or the material may sublimate directly on heating. With ablation cleaning techniques, if damage to the treatment surface is to be prevented, the ablation energy must be exactly aimed toward contaminants rather than toward the surface on which the contaminants lie, a difficult task when the contaminants are extremely small or randomly spaced. Even where the ablation energy can be successfully directed at a contaminant, it is difficult to vaporize the contaminant without also damaging the underlying treatment surface.

Surface cleaning by melting, annealing, and thermal ablation can be conducted with a laser energy source. However, using a laser energy source to remove contaminants from a surface by melting, annealing or thermal ablation does not overcome the inherent disadvantages or these processes. For example, in U.S. Pat. No. 4,292,093, "Method Using Laser Irradiation For the Production of Atomically Clean Crystalline Silicon and Germanium Surface," the laser annealing method disclosed requires both vacuum conditions and energy levels sufficient to cause rearrangement and melting of the treatment surface. Other known laser surface cleaning methods involving melting or annealing require similar high energy lasing and/or vacuum conditions, as disclosed in U.S. Pat. Nos. 4,181,538 and 4,680,616. The method of U.S. Pat. No. 3,464,534 suffers the same drawbacks as other high energy laser thermal ablation methods.

The method of U.S. Pat. No. 4,980,536 to Asch et al. uses a high power density excimer laser pulse directed to both front and back sides of a mask to remove small particles. The method of U.S. Pat. No. 4,987,286 to Allen uses an energy transfer medium interposed between each particle to be removed and the surface to which the particles are adhered. The method of U.S. Pat. Nos. 5,283,417 and 5,393,957 to Misawa et al. uses two lasers, a pulsed laser and a trapping laser, to perform modification and processing of particles and microcapsules. The method of U.S. Pat. No. 5,332,879 to Radhakrishnan et al. for removing trace metal contaminants from organic dielectrics such as polyimide uses pulsed ultraviolet radiation to remove the contaminants by a process of ablation. The method of U.S. Pat. No. 5,637,245 to Shelton et al uses a laser for cleaning equipment surfaces and provides a barrier layer at the surface to be cleaned. The barrier layer ensures that energy from the laser light is evenly distributed and shields the surface from oxygen to prevent oxidation of the surface.

**Objects and Advantages of Invention**

A first major object or purpose of the invention is a system for enhancing test yield in semiconductor manufacturing. A second object is a set of methods that enables enhanced test yield in semiconductor manufacturing. A related object is a system that integrates particularly effective cleaning methods into manufacturing tooling for achieving extremely low defect densities, especially for very small particulate defects that affect test yield of semiconductor products characterized by extremely fine minimum dimensions. A further related object is a system that is capable of locating, identifying, and removing individual defects of various sizes, shapes, and compositions from wafer surfaces at various stages in the wafers' fabrication. A still further related object is a system that is capable of individually locating, identifying, and removing those particular individual defects that are "killer" defects, i.e. those defects that, because of their nature, size, and location at critical portions of a semiconductor product design, would adversely affect device functionality or performance. To achieve these objects, a more practical object is a system that incorporates cleaning apparatus and methods capable of area cleaning of wafers and also capable of local removal of individual particulates from wafers. A more detailed object is a system including means for transferring semiconductor wafers among a number of processing stations under program control and for creating and maintaining a data record for each wafer indicating processing results at each processing station, also including means for performing a wafer surface cleaning of defects using a photon flux process followed by vapor cleansing, and also including means for transferring cleaned wafers to an output station. Another detailed object is a method for processing wafers including the steps of transferring each wafer to a number of processing stations in a predetermined sequence starting at an input station and ending at an output station, creating and maintaining a data record at each of the stations, mapping and recording the locations of defects on each wafer, cleaning defects from each wafer using a photon flux process followed by vapor cleansing, and transfering the wafers to an output station. These and other objects, features, and advantages will be apparent from a reading of the following description, along with the accompanying drawings and the appended claims.

**Disclosure f Invention**

This invention is a technology tool that will eradicate defects in order to achieve the very low defect levels required, even as the industry produces finer and finer feature sizes. An improved semiconductor wafer processing apparatus includes a series of processing stations, in one form, coupled together by computer-controlled cluster tooling which is programmed to achieve a selected wafer throughput for the apparatus at a selected defect level in the range of at least 0.01 defects/$cm^2$. Wafers are supplied in a pod to an input station which initiates a data record for recording wafer processing results at each processing station and transfers individual wafers to a precleaning station under control of the wafer handling equipment. The pre-cleaning station performs a self-directed vacuum bake for each wafer after which the pod is transferred to a self-directed defect mapping station where wafer surface defects are identified and located in their x-y coordinates. The defect-mapped wafers are transferred to a self-directed (i.e., computer-controlled) laser area cleaning station which lifts the defects and sweeps the wafer surface clean, except for stubborn defects. Clean wafers are transferred to a final mapping station where the wafer record is updated, followed by transfer of the wafers to an output station. Wafers including stubborn defects are transferred to a second wafer defect mapping station where the stubborn defects are located in x-y coordinates, after which those wafers are transferred to a self-directed (i.e., computer-controlled) Defect Review Tool incorporating a Scanning Electron Microscope (SEM-DRT). An ultra high power wafer surface SEM image review of stubborn defects is performed including a chemical analysis (by energy-dispersive spectroscopy) of the stubborn defects, after which the wafers are routed to a self-directed (i.e., computer-controlled) laser point cleaning station which addresses each stubborn defect identified by x-y coordinates denoted in the data record accompanying the wafer. The laser point cleaning station performs a defect removal operation by lifting and sweeping each stubborn defect from the wafer surface followed by transferring the cleaned wafers to a third wafer defect mapping station where any stubborn defects remaining are mapped in x-y coordinates and recorded in the accompanying data record, after which these wafers are transferred to a second laser area cleaning station. A final cleaning is performed at the second laser cleaning station followed by transfer of the wafers to a final mapping station for location

in x-y coordinates of any remaining stubborn defects. The accompanying data records for the wafers are updated. Finally, the wafers are transferred to the output station.

**Brief Description of Drawings**

Figure 1 is a plan view of manufacturing apparatus incorporating the principles of the present invention of defect eradication on semiconductor wafers.

Figure 2 is a flow chart illustrating the steps of a manufacturing method performed in accordance with the invention.

Figure 3 is a plan view of a simplified manufacturing apparatus incorporating the principles of the present invention.

Figure 4 is a plan view of another simplified manufacturing apparatus incorporating the principles of the present invention.

Figure 5 is a graph illustrating a conventional S-shaped yield learning curve commonly occurring in semiconductor fabrication.

**Modes for Carrying Out the Invention**

Description of Preferred Embodiment

The invention employs a process (hereafter "Radiance Process"), described in U.S. Pat. No. 5,024,968 to Engelsberg et al., which is based upon the principles of quantum physics rather than chemistry for wafer cleaning purposes. Related methods are described in U.S. Pat. Nos. 5,099,557, 5,531,857, and 5,643,472 to Engelsberg et al. The entire disclosures of U.S. Pat. Nos. 5,024,968, 5,099,557, 5,531,857, and 5,643,472 are incorporated herein by reference. As used in the present invention, the Radiance Process comprises of two components:

(1) A photon flux is applied to the surface to be cleaned. This is usually from a deep ultraviolet excimer laser, but Nd:YAG or $CO_2$ lasers are sometimes suitable. The light source and energy and power fluxes are determined by the combination of surface and contaminant. The photon flux provides sufficient energy to break the bonds holding

contaminants to a surface. There is currently no predictive model for processing parameters or any agreed upon mechanism by which the process operates. The mechanism has been variously described in terms of interactions including: photodissociation, phonon shock, photophoresis, photon-phonon interaction, acoustic stress waves, or quasi-metastable states. As the photon energy is transferred to the surface-contaminant bonds, bonds break and the contaminants rise above the surface.

(2) To prevent recontamination and the emission of particulate contaminants into the work area surrounding the wafer, the contaminants must be removed from the work area. This is accomplished by the use of a flowing gas, usually in a laminar regime to provide a stable boundary layer. The gas, usually nitrogen or argon, must be chosen so as to obviate reactions between it and the surface, noting the photocatalytic effect of some forms of photon flux. The gas may have a role in the process of ejecting the contaminants once they are free of the surface.

Depending upon tool configuration, the process may be applied to a variety of surface configurations ranging from flat surfaces to irregular broken crystals. Processing speed is largely determined by the choice of a particular light source. Process optimization involves tradeoffs of speed, cost, tool size, tool components and operator involvement. There appears to be a range of processing parameters which can produce the desired cleaning for most applications.

The apparatus and method will be described first in terms of a preferred embodiment intended for a complete "high-end" or generic system for use in the earliest stage of a typical semiconductor test yield improvement curve. This earliest regime is indicated by roman numeral I in FIG. 5. A simplified "mid-range" system is then described for use in the intermediate (rapid test-yield-improvement) stage indicated by roman numeral II in FIG. 5. A further simplified "low-end" system is most useful in the latest (high test yield) stage indicated by roman numeral III of FIG. 5. While FIG. 5 shows dashed dividing lines between the regimes I, II, and III at approximately 20% and 80% test yield, there is no special quantitative significance to those test yield levels. The test yields at which a transition is made between the three indicated regimes are somewhat arbitrary and may vary with the particular semiconductor product and/or fabrication

process. Thus the dividing line between regimes I and II may vary from about 5% test yield to about 30% test yield, for example, with similar variations for the transition from regime II to regime III.

Figure 1 shows a generic defect eradicator system **10**, nicknamed MIDAS or YES (Yield Enhancement System), that utilizes laser cleaning technology and wafer defect mapping technology/tooling/SEM defect revenue tooling and a cluster tooling main frame architecture. The system elements include the following: area laser cleaner station **11, 12** and laser point cleaner station **13**, which may be apparatus manufactured by Radiance Services Company, Bethesda, Maryland; wafer mappers **18 - 22**, which may be apparatus manufactured by KLA, 160 San Roblas, San Jose, California; Scanning Electron Microscope - Defect Review Tool (SEM-DRT) **24**, which may be apparatus manufactured by Amray, 160 Middlesex Turnpike, Bedford, Massachusetts; and computer-controlled cluster tooling **26** for wafer handling purposes including input and output ports **28, 30** respectively, which may be apparatus manufactured by Applied Materials, 350 Bowers Avenue, Santa Clara, California. Optionally, the cluster tooling may include a wafer pre-clean station **34**. Laser cleaner stations utilize the Radiance Processes described in the U.S. Pat. Nos. 5,024,968, 5,099,557, 5,531,857, and 5,643,472. Curved arrows in FIGS 1, 3, and 4 show schematically the movement of wafers from station to station. The wafer yield enhancement/improvement system described in the following description will eradicate in-line IC defects and thereby increase IC yields and dramatically increase the individual wafer revenue potential by using the following process in the overall apparatus **10**. Most of the stations of FIGS. 1, 3, and 4 operate with gas atmospheres such as clean air. As is known in the art, some of the stations (e.g., wafer pre-clean station **34** and SEM-DRT **24**) require vacuum for their operation, and therefore require conventional airlock interfaces.

The overall process comprises the steps shown schematically in FIG. 2. Specific steps are denoted by reference numerals **S1** ... **S12**. Wafers coming to the system in a pod of wafers (not shown) are processed in the following manner:

(1) Wafer pod loaded (**S1**) at input station **28**.

(2) Optionally, wafers are processed (**S2**) one by one at a pre-clean station **34** (vacuum

bake station).

(3) Wafers are moved to a wafer mapper station **14**. Wafers are mapped (**S3**) for defects and their x-y positions (positional coordinates).

(4) Wafers are illuminated one-by-one by an excimer laser and are swept clean (**S4**) with nitrogen gas in a laser area cleaning station **11**.

(5) Wavers now are subject to optionally being directed to

(a) final wafer mapper **22** (**S5**) and output (**S12**) ("clean" wafers) at output station **30**; or

(b) on to wafer mapper **16** ("partially clean" wafers)(**S6**).

(6) Wafers can then be routed to SEM Defect Review Tool Station **24** for ultra high power image review and also a chemical analysis (**S7**). This stage will be used for extremely "stubborn" defects.

(7) The wafers are then routed to the Laser-Point Clean station **13**. Individual defect locations are addressed and the laser is directed to each x/y location to point clean each individual defect (**S8**).

(8) The wafers are then re-mapped (**S9**) at station **18**.

(9) The wafers are then directed to laser area clean station **12** where the final area clean of the wafers is performed (**S10**).

(10) The wafers are then mapped (**S11**) at station **20** and outputted (**S12**) at output station **30,** where the wafers are extremely clean compared with incoming wafers (pre-Midas) and will exhibit dramatically increased wafer yields.

The wafer cleaning apparatus of area laser cleaner station **11, 12** and laser point cleaner station **13,** and the cleaning methods employed may be similar to those described in U.S. Pat. Nos. 5,024,968, 5,099,557, 5,531,857, and 5,643,472 (each incorporated by reference). The specific apparatus details are shown in the descriptions and drawings of those patents and are not repeated in FIGS. 1 - 5 of the present application. Similar methods are also described in the articles by A. Engelsberg, "Particle Removal from Semiconductor Surfaces Using a Photon-Assisted, Gas-Phase Cleaning Process," Materials Research Society Symposium Proceedings, vol. 315, pp. 255-260, (1993) and "Laser-Assisted Cleaning Proves Promising" Precision Cleaning, May 1995.

An assembly holds a substrate (e.g., semiconductor wafer) from which surface particulate defects are to be removed. A gas from a gas source is constantly flowed over the wafer. The gas is inert to the wafer and is flowed across the wafer so as to bathe the wafer in a non-reactive gas environment. Preferably, the gas is a chemically inert gas such as helium, nitrogen or argon. An enclosure for holding the wafer communicates with a gas source through a series of tubes, valves, and a gas flow meter. The enclosure preferably comprises a stainless steel reaction cell fitted with opposing gas inlet and outlet ports. The enclosure is fitted with a sealed optical grade quartz window or light guide (e.g., a suitable fiber-optic light guide) through which the radiation can pass, or the laser could be placed within the enclosure. The inlet and outlet ports may comprise, for example, stainless steel tubing fitted with valves. After the wafer is transported into the enclosure, the enclosure is repeatedly flushed and backfilled with the gas and is kept at a pressure slightly above ambient atmospheric pressure to prevent inflow of other gases. Flow of the gas may be regulated by a flow meter such as a Matheson Model 602 flow meter. The valves are preferably metering valves, regulating valves, or bellows valves suitable for high temperature and pressure applications and for use with toxic, hazardous, corrosive or expensive gases or liquids, as for example Swagelok SS-4H sup TM series valves by Swagelok Co. of Solon, Oh.

Each wafer is irradiated with high-energy irradiation characterized by an energy density and duration between that required to release surface contaminants from the substrate treatment surface and that required to alter the crystal structure of the substrate treatment surface. According to the preferred embodiment, a laser generates laser irradiation which is directed against the wafer surface. The energy flux and the wavelength of the high-energy irradiation is preferably selected to be dependent upon the surface defects being removed. To this end, a gas analyzer may be connected to area laser cleaner station **11**, **12** and laser point cleaner station **13**. The gas analyzer analyzes the contents of exhaust gas from the enclosure to facilitate selective energy and wavelength adjustment of the laser. The gas analyzer may be a mass spectrometer as, for example, a quadrapole mass spectrometer manufactured by Bruker Instruments, Inc. of Billerica, Mass. or by Perkin Elmer of Eden Prairie, Minn.

Selection of the high-energy irradiation source for use in the invention depends upon the desired irradiation energy and wavelength. The electron volt/photon (eV/photon) of the irradiation is preferably at least twice the energy necessary to break the bonds adhering the particulate contaminants to the surface being cleaned. The bond energies between common contaminants such as particulates composed of compounds of carbon, hydrogen and oxygen, and common substrate materials such as silicon, titanium, germanium, iron, platinum and aluminum range between 2 and 7 eV/bond as disclosed in Handbook of Chemistry and Physics, 68th ed., pp. F-169 to F-177 (CRC Press 1987) which is hereby incorporated by reference. Accordingly, lasers emitting photons with energies in the range of 4 to 14 eV/photons are desirable. The wavelength should be below the wavelength that would compromise the integrity of the substrate surface by the photoelectric effect, as described in G. W. Castellan, Physical Chemistry, 2nd ed., 458-459 (Academic Press, 1975) which is hereby incorporated by reference. The preferred wavelength depends on the molecular species being removed and the resonance states of such species. The wavelengths and photon energies of a number of lasers operable in the invention are listed in Table 1 of U.S. Pat. Nos. 5,024,968 and 5,531,857, and Table 1c of U.S. Pat. No. 5,643,472. A number of those lasers are described in greater detail in the following references which are hereby incorporated by reference: M. J. Webber, ed., CRC Handbook of Laser Science, Vols. 1-5 (1982-1987); Mitsuo Maeda, Laser Dyes, (Academic Press 1984); and laser product literature from Lambda Physik at 289 Great Road, Acton, Mass. Coherent, Inc. at 3210 Porter Drive, Palo Alto, Calif. and Spectra-Physics at 1250 West Middlefield Road, Mountain View, Calif. It is anticipated that high-energy xenon or mercury lamps or other types of lasers, including visible, ultraviolet, infrared, x-ray or free electron lasers might be utilized as the irradiation source in the present invention. The irradiation energy density and duration of irradiation used is such that the heat of formation is not approached on the wafer surface. Finding the maximum energy usable on a given wafer material will require some experimentation in light of the material's known heat of formation. Thus, annealing, thermal ablation, and melting are prevented from occurring. When a wafer surface is irradiated as described above, the bonds and/or forces holding particulate defects to the substrate surface are broken and the

inert carrier gas carries contaminants away from the substrate surface during laser irradiation. As long as the cleaned substrate remains in the inert gas environment, new contaminants will not form on the substrate surface. If necessary, a suitable trapping system may be connected to apparatus **10** (preferably at laser area clean stations **11** and **12** and laser pin-point clean station **13**) for trapping and neutralizing removed contaminant species.

The wafers being treated may be selectively exposed to the laser irradiation by a variety of methods. For example, the wafer may be fixed on an X-Y table which is selectively moved with respect to a fixed beam of laser pulses that are directed through a beam splitter and a focusing lens before contacting selected portions of the surface of the wafer over which inert gas flows. Alternatively, laser pulses may be split by beam splitters into two sets of pulses which are selectively moved by adjusting mirrors over the surface of the wafer on a fixed table. A laser power meter allows for close monitoring of the laser power being applied to the wafers. In general, the photons are preferably directed perpendicular to the plane of the portion of the wafer being treated, to maximize the power and energy fluxes at the surface for a given output from the source of photons. However, the photons may be directed at an angle to the wafer as convenient or necessary for implementation of the process. In some situations, it may be preferable to direct the radiation at an oblique angle to the wafer. Of course, the energy and power fluxes at the surface will vary with the angle of incidence of the photons with respect to the plane of the surface, and this variation must be taken into account in selecting the output of the photon source.

Figure 1 shows an integrated system that incorporates all four tool elements. However, the four system elements may also be separated into individual "tools." Wafers would then be transported between the individual Midas Tool elements by using a mini-environment pod. Simplified configuration versions of the integrated system are shown in Figures 3 and 4. Figure 3 is a plan view of a simplified "mid-range" manufacturing apparatus for use in the intermediate (rapid yield-improvement) stage of a typical semiconductor manufacturing process yield-improvement curve. Figure 4 is a plan view of a further simplified "low-end" manufacturing apparatus for use in the latest (high

yield) stage of a typical semiconductor manufacturing process yield-improvement curve.

Thus, one important aspect of the invention is an improved semiconductor wafer processing apparatus that includes a series of processing stations, in one form, coupled together by computer-controlled cluster tooling which is programmed to achieve a selected wafer throughput for the apparatus at a selected defect level in the range of at least 0.01 defects/$cm^2$. Wafers are supplied in a pod to an input station which initiates a data record for recording wafer processing results at each processing station. The individual wafers are transferred to a self-directed defect mapping station where wafer surface defects are identified and located in their x-y coordinates. The defect mapped wafers are transferred to a self-directed laser area cleaning station which lifts the defects and sweeps the wafer surface clean, except for stubborn defects. Clean wafers are transferred to a final mapping station where the wafer record is updated, followed by transfer of the wafers to an output station. Wafers including stubborn defects are transferred to a second wafer defect mapping station where the stubborn defects are located in x-y coordinates, after which the wafers are transferred to a self-directed Defect Review Tool incorporating a Scanning Electron Microscope (SEM-DRT). An ultra high power wafer surface SEM image review of stubborn defects is performed including a chemical analysis of the stubborn defects, after which the wafers are routed to a self-directed laser point cleaning station which addresses each stubborn defect identified by x-y coordinates denoted in the data record accompanying the wafer. Optionally, the physical and/or chemical characteristics of each defect may be used for defect classification. Computer software programmed to perform automatic defect classification (ADC) is commercially available. The laser point cleaning station performs a defect removal operation by lifting and sweeping each stubborn defect from the wafer surface followed by transferring the cleaned wafers to a third wafer defect mapping station where any stubborn defects remaining are mapped in x-y coordinates and recorded in the accompanying data record, after which the wafers are transferred to a second laser area cleaning station wafer. A final cleaning is performed at the second laser area cleaning station followed by transfer of the wafers to a final mapping station for location in x-y coordinates of any remaining stubborn defects. The accompanying data records for the wafers are updated followed by transfer of the wafers to the output station.

As mentioned above, it is known that not all particulates are equally undesirable. For example, particulates that adhere at some non-sensitive portions of the IC circuitry may have no effect on operation or performance, and need not necessarily be removed ("don't cares" or "cosmetic" defects). Similarly, defects having innocuous physical and/or chemical characteristics may be cosmetic defects. On the other hand, particulates that adhere at locations where they would be critical to device operation ("killer defects") can cause test failure of the IC circuitry and must be removed for proper operation. Each mapped defect may optionally be further characterized by automatic defect classification, as its physical and chemical characteristics may be pertinent to whether the defect is a killer defect. The present invention is adaptable for selective removal of only killer defects. The positional coordinates of mapped defects are compared (by computer software) with device design data for identifying the killer defects critical to device operation, and the photon flux is then selectively applied only at the positional coordinates of the killer defects while ignoring other defects.

**Example**

The following example illustrates the potential dramatic wafer revenue increase for a system on a chip (SOC) IC product with an average sale price (ASP) of $1,000. The SOC product is assumed to have 0.18 micron minimum feature size and 30 mask levels, 22 of them non-critical with 0.25 micrometer minimum feature size, and 8 of them critical with 0.18 micrometer minimum feature size. With a wafer diameter of 300 mm, the total number of 800 $mm^2$ SOC chips per wafer is 70. With the apparatus and methods of the present invention reducing the defect level to 0.008 defects/$cm^2$ and thus improving the test yield by 3% from 70% to 73%, the added revenue is estimated at $2,000 per wafer. For 25,000 wafer starts per month per fabrication facility, the total added revenue produced by one fabrication facility would be $600 million per year.

MIDAS IC Yield System Improvements

Wafer Revenue Adder

Example:

- 1000 MIP System on a Chip (SOC)
- Circa 2001
- 0.18 Micron Technology
- 300 mm Wafers
- 30 Mask Levels
- 22 Non-Critical - 0.25 micrometer minimum feature size
- 8 Critical - 0.18 micrometer minimum feature size
- 800 $mm^2$ Chip Size
- 70 SOC Dice/wafer

| | **Do** | **Wafer Test Yield** |
|---|---|---|
| SIA (0.18 micrometer) Defect Target | 0.010 Defect/$cm^2$ (Wet Cleaned Wafer) | 70% |
| Defect shortfall | 0.030 Defect/$cm^2$ | 28% |
| Defect shortfall | 0.055 Defect/$cm^2$ | 13% |

Midas/Radiance Clean Wafers

Laser Cleaned Wafers - "Cleaner" than Wet Cleaned Wafers

Midas* Reduced Defect Level 0.008 D/cm2 = 73%

* Midas - Defect eradication system made in accordance with the present invention

- 70 SOC Chips/300 mm Wafers
- Assume ASP = $1,000/SOC

Midas/RC Process:

| | | | | |
|---|---|---|---|---|
| 73% | = | 51 Chips | = | $51,000/wafer |
| 70 % | = | 49 Chips | = | $49,000/wafer |
| 28% | = | 20 Chips | = | $20,000/wafer |
| 13 % | = | 9 Chips | = | $9,000/wafer |

Therefore: Midas RC (Radiance) Process = $2,000/Wafer Revenue Adder

Assume: 25,000 Wafer (300 mm) starts/month/Fab

Therefore: Midas/RC (Radiance) Process = $50M+ /Month /Fab

In one year (e.g., 2001), one 300 mm Midas/RC (Radiance) SOC Laser Clean Technology Fab will generate +$600M Δ[Delta] revenue over a non-RC (non-Radiance) wet clean Fab

**Industrial Applicability**

A manufacturing apparatus made in accordance with the invention is applicable to manufacturing processes that require extremely low defect densities, especially semiconductor wafer and photomask fabrication processes. The methods of the invention can be used to reduce defect densities of semiconductor wafers, thus increasing the yields and lowering the costs of the semiconductor products on the wafers. Similar apparatus suitably arranged can be used in the manufacture of masks, such as glass or quartz photolithography masks or membrane masks used for photolithography, X-ray lithography, electron projection lithography, or ion-projection lithography.

While the invention has been shown and described in connection with a preferred embodiment, various changes may be made therein without departing from the spirit and scope of the invention as defined in the appended claims. For example, various combinations of elements can be clustered in arrangements other than those shown, with suitable process sequences for moving wafers from one element to another. The order of steps of the processes may, of course, be varied.

What is claimed is:

## CLAIMS

1. An improved semiconductor wafer processing apparatus with defect eradication comprising:

a) means for transferring a plurality of semiconductor wafer among a plurality of processing stations under program control and for creating and maintaining a data record for each wafer indicating processing results at each processing station;

b) means for performing a wafer surface cleaning of defects using a photon flux process followed by vapor cleansing; and

c) means for transferring of cleaned wafers to an output station.

2. Apparatus as recited in claim 1, further comprising:

d) means for mapping position coordinates of surface defects on each wafer and for recording the coordinates in said data record.

3. Apparatus as recited in claim 2, further comprising:

e) means for identifying and locating stubborn defects with respect to their position coordinates and for updating said data records for any surface cleaned wafers.

4. Apparatus as recited in claim 3, further comprising:

f) means for performing an elemental chemical analysis of said defects to identify any extremely stubborn defects.

5. Apparatus as recited in claim 4, further comprising:

g) means for performing a point cleaning of stubborn defects by said position coordinates using said photon flux process followed by vapor cleansing.

6. Apparatus as recited in claim 1, further comprising:

h) means for performing a final mapping and data record update of wafer surface defects in position coordinates before transfer of the cleaned wafers to said output station.

7. An improved semiconductor wafer processing apparatus with defect eradication comprising:

a) means for transferring a plurality of semiconductor wafer among a plurality of processing stations under program control and for creating and maintaining a data record for each wafer indicating processing results at each processing station;

b) means for mapping surface defects in x-y coordinates for each wafer and recording the coordinates in the accompanying data record;

c) means for performing a wafer surface cleaning of defects using a photon flux process followed by vapor cleansing;

d) means for identifying and locating stubborn defects in x-y coordinates and for updating accompanying data records for any surface cleaned wafers;

e) means for performing an elemental chemical analysis of to identify any extremely stubborn defects;

f) means for performing a point cleaning of stubborn defects by x-y coordinates using the process of step (c);

g) means for performing a final wafer surface cleaning using the process of step (c); and

h) means for performing a final mapping and data record update of wafer surface defects in x-y coordinates using the process of step (b) followed by transfer of the cleaned wafers to an output station.

8. The apparatus of Claim 7 further comprising:

i) means for removing wafers without stubborn defects after step (c) for a final defect mapping and transfer to the output station.

9. A method for processing semiconductor wafers comprising the steps of:

(a) transferring each wafer to a plurality of processing stations in a predetermined sequence starting at an input station and ending at an output station;

(b) creating and maintaining a data record of the results of processing each wafer at each of said stations;

(c) mapping surface defects in positional coordinates for each wafer at at least one of said stations, and recording said coordinates in the accompanying data record;

(d) performing a wafer surface cleaning of defects using a photon flux process followed by vapor cleansing at at least one of said stations; and

(e) transferring said wafers to said output station for completion of said processing.

10. A process as recited in claim 9, further comprising the step of:

(f) identifying and locating stubborn defects at their respective positional coordinates and

updating accompanying data records for any surface cleaned wafers.

11. A process as recited in claim 9, further comprising the step of::

(g) identifying and locating stubborn defects in their respective positional coordinates and

updating accompanying data records for any surface cleaned wafers.

12. A process as recited in claim 10 wherein said identifying and locating said stubborn defects is a final identifying and locating of said defects.

13. A process as recited in claim 10 wherein said identifying and locating said stubborn

defects is performed by scanning electron microscopy of said defects.

14. A process as recited in claim 10 wherein said identifying and locating said stubborn defects is performed by optical microscopy of said defects.

15. A process as recited in claim 10 wherein said wafer surface cleaning of defects is performed by selectively aiming said photon flux at said stubborn defects.

16. A process as recited in claim 15 wherein said photon flux is selectively applied only at said positional coordinates of defects expected to affect device yield.

17. A process as recited in claim 16 wherein each set of said positional coordinates is obtained from said accompanying data records.

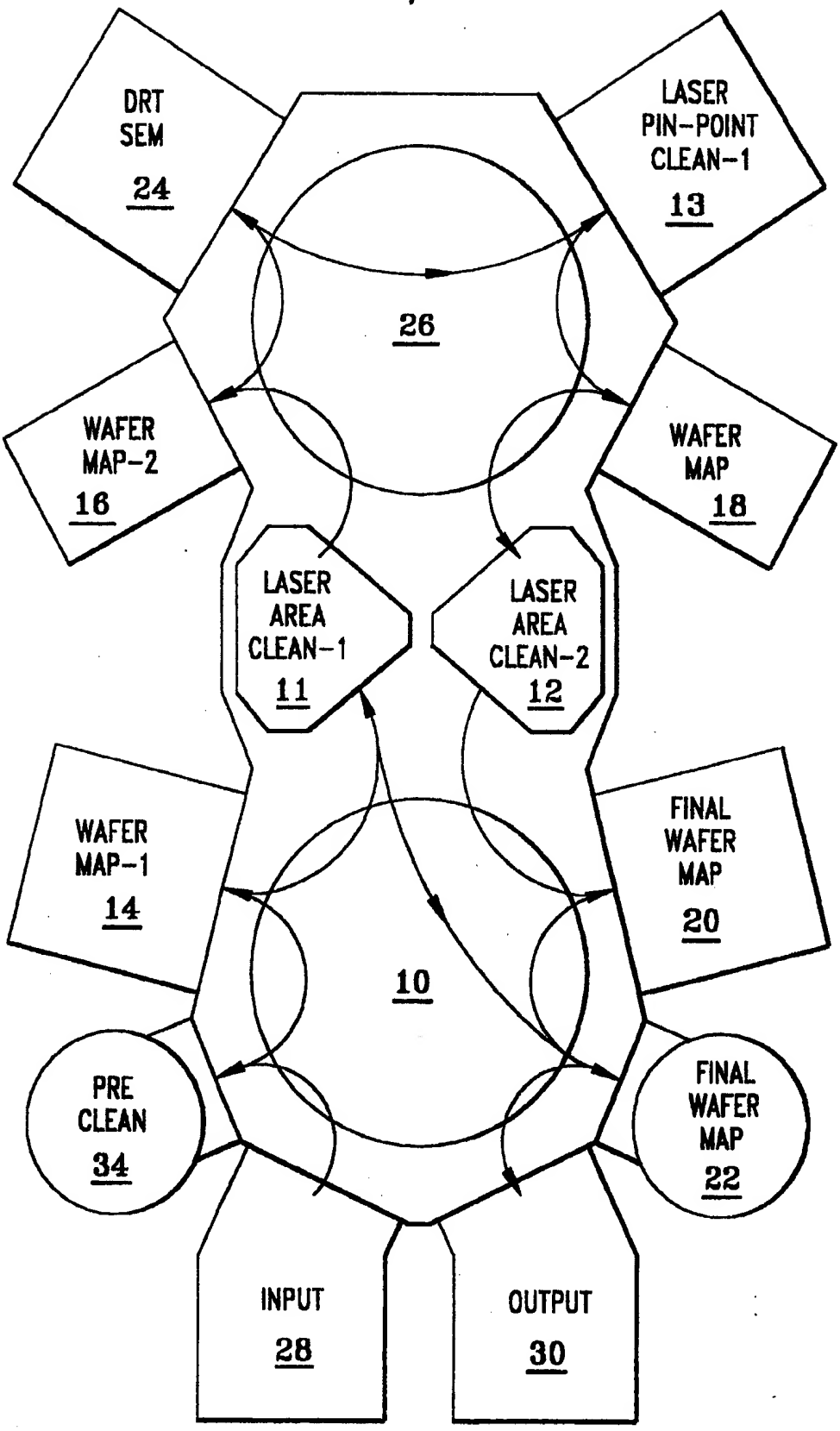
18. A process as recited in claim 9, further comprising the step of:

(h) comparing said positional coordinates mapped in step (c) with device design data for identifying defects critical to device operation.

19. A process as recited in claim 15, further comprising the step of:

(h) comparing said positional coordinates mapped in step (c) with device design data for identifying defects critical to device operation,

wherein said photon flux is selectively applied only at said positional coordinates of said defects critical to device operation while ignoring other defects.


DRT
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LASER
PIN-POINT
CLEAN-1
13
26
WAFER
MAP-2
16
WAFER
MAP
18
LASER
AREA
CLEAN-1
11
LASER
AREA
CLEAN-2
12
WAFER
MAP-1
14
FINAL
WAFER
MAP
20
10
PRE
CLEAN
34
FINAL
WAFER
MAP
22
INPUT
28
OUTPUT
30

FIG. 1

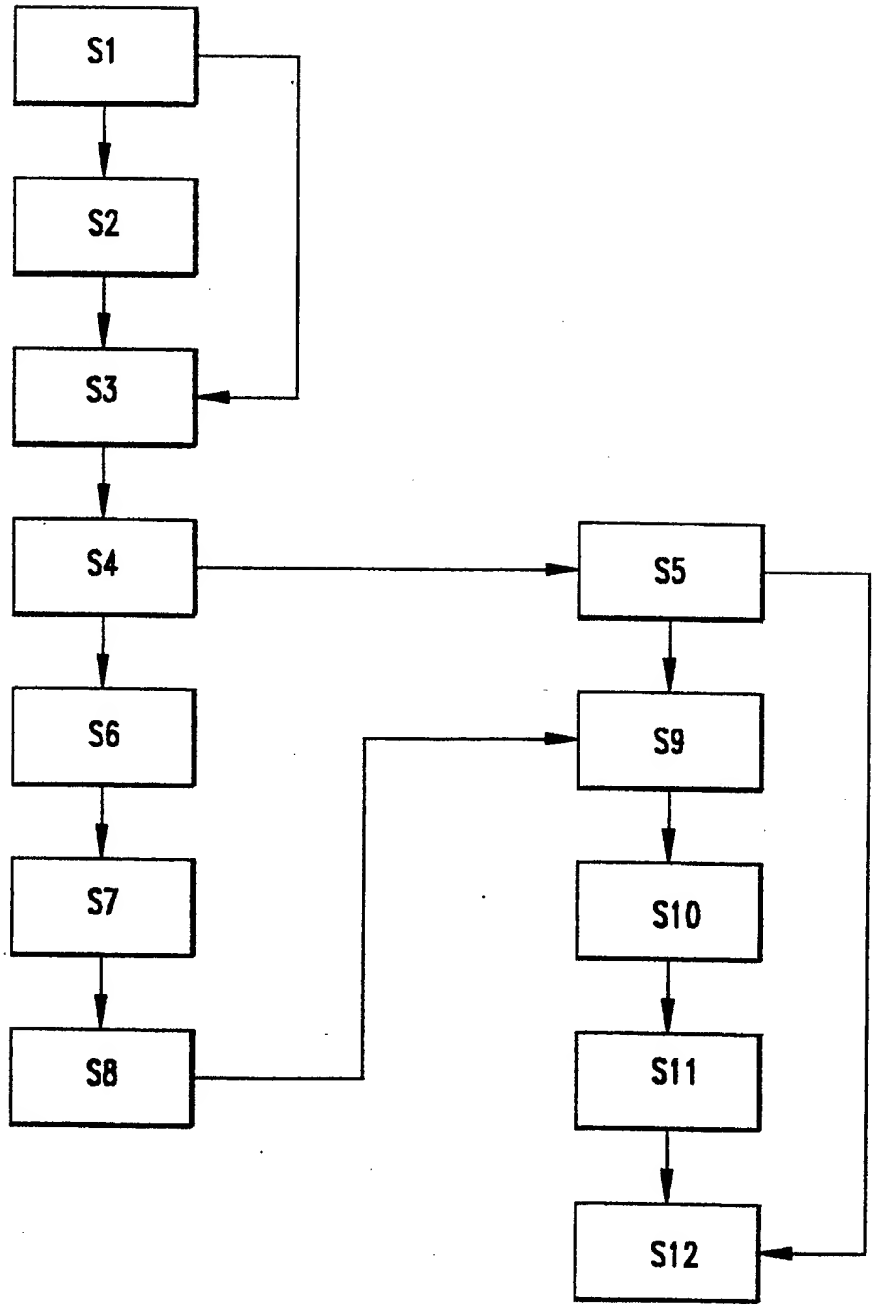


FIG. 2

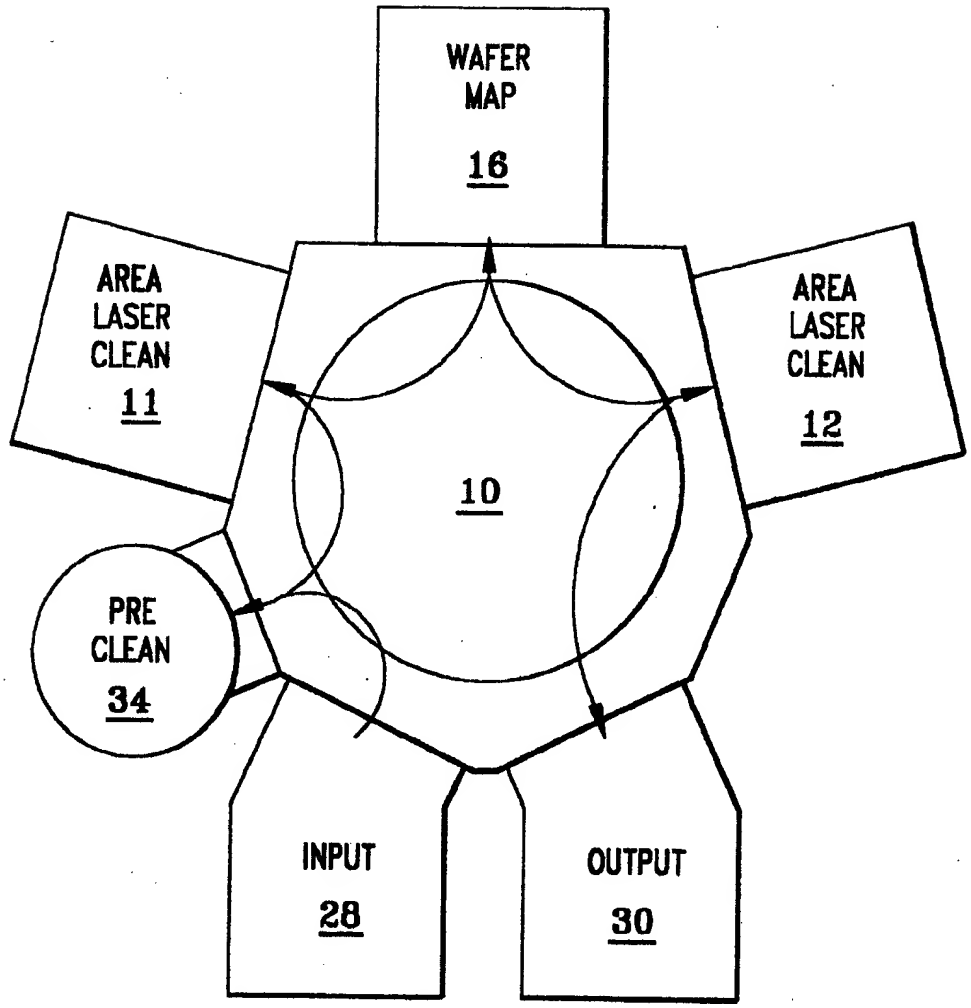
WAFER MAP
16
AREA LASER CLEAN
11
AREA LASER CLEAN
12
10
PRE CLEAN
34
INPUT
28
OUTPUT
30

FIG. 3

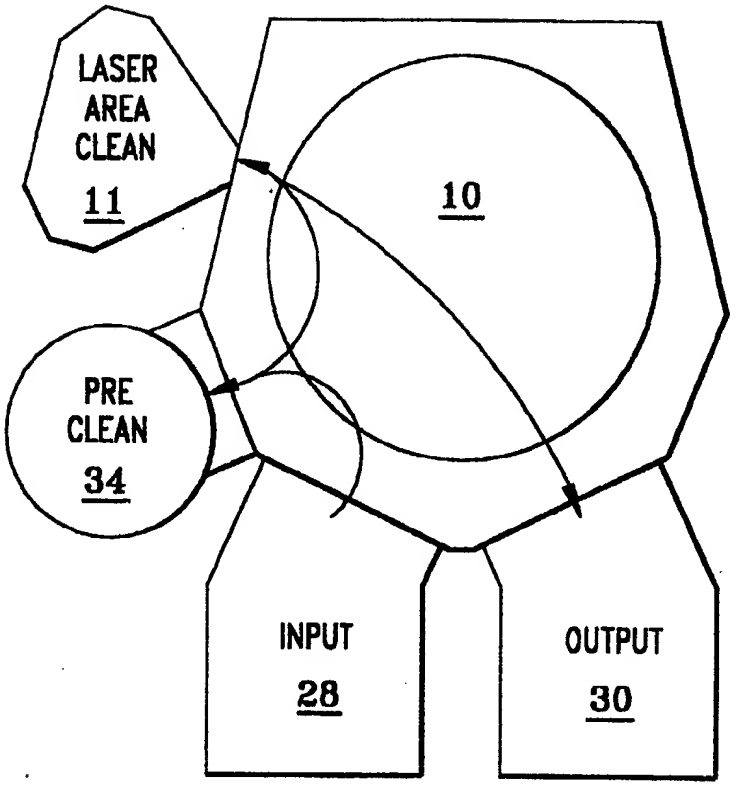
LASER
AREA
CLEAN
11
10
PRE
CLEAN
34
INPUT
28
OUTPUT
30

FIG. 4

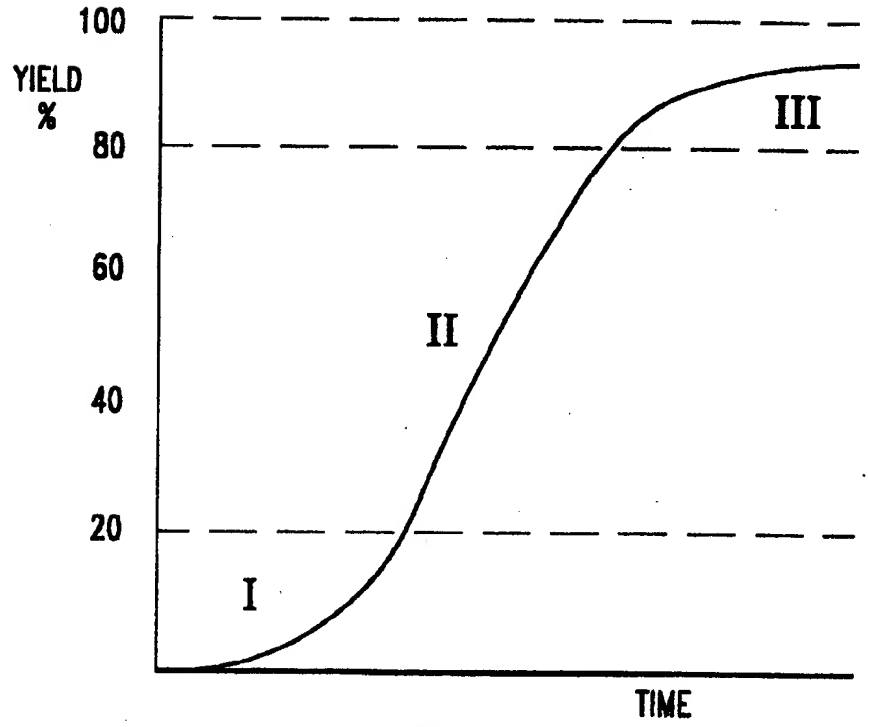
100
YIELD
%
80
60
40
20
I
II
III
TIME

FIG. 5